WHAT IS CLAIMED IS:

1. A method for processing a semiconductor topography, comprising:

polishing an upper layer of the semiconductor topography to expose a first underlying layer;

etching away remaining portions of said first underlying layer to expose a second underlying layer; and

subsequently planarizing the topography.

2. The method of claim 1, wherein said polishing the upper layer comprises removing portions of the upper layer arranged above the upper surface of the first underlying layer.

3. The method of claim 1, wherein said polishing the upper layer of the topography comprises polishing a portion of the first underlying layer.

4. The method of claim 3, wherein a thickness of the first underlying layer is sufficient to prevent polishing through the first underlying layer during said polishing the upper layer.

5. The method of claim 1, further comprising forming the upper layer, first underlying layer, and second underlying layer upon a semiconductor layer and in a single process chamber.

6. The method of claim 1, further comprising depositing the upper layer within a trench of the semiconductor topography prior to said polishing.

7. The method of claim 6, wherein said polishing the upper layer comprises polishing the upper layer such that remaining portions of the upper layer are laterally confined by sidewalls of the trench.

8. The method of claim 1, further comprising etching the planarized topography such that a third underlying layer is removed, wherein the third underlying layer is arranged beneath the second underlying layer.

9. The method of claim 8, wherein etching the planarized topography comprises removing a portion of the second underlying layer.

10. A method for fabricating shallow trench isolation regions, comprising:

forming one or more trenches extending through a stack of at least three layers arranged over a semiconductor substrate, wherein the stack comprises intervening layers of different etching characteristics;

blanket depositing a dielectric over the trenches and the stack of layers such that the trenches are filled by the dielectric; and

planarizing the dielectric such that upper surfaces of the dielectric remaining within the trenches are coplanar with an upper surface of an adjacent layer of the stack, wherein said planarizing comprises removing one or more layers of the stack.

11. The method of claim 10, wherein said planarizing comprises:

polishing the dielectric to expose an upper layer of the stack;

etching the upper layer to expose an intermediate layer of the stack; and

subsequently polishing the topography to expose the upper surface of the adjacent layer of the stack.

12. The method of claim 11, wherein said subsequently polishing the topography is sufficient to produce a substantially planar surface without dishing portions of the adjacent layer.

13. The method of claim 11, wherein a thickness of said upper layer is between approximately 500 angstroms and approximately 1000 angstroms prior to said planarizing.

14. The method of claim 11, wherein said upper layer comprises silicon nitride.

15. The method of claim 11, wherein a thickness of said intermediate layer is between approximately 300 angstroms and approximately 700 angstroms prior to said planarizing.

16. The method of claim 11, wherein said intermediate layer comprises silicon dioxide.

17. The method of claim 11, wherein said intermediate layer and said dielectric comprise similar etch characteristics.

18. The method of claim 11, wherein said adjacent layer comprises the intermediate layer.

19. The method of claim 11, wherein said adjacent layer comprises a lower layer of the stack.

20. The method of claim 19, wherein a thickness of said lower layer is between approximately 300 angstroms and approximately 500 angstroms prior to said planarizing.

21. The method of claim 19, wherein said lower layer comprises silicon nitride.

22. The method of claim 10, further comprising etching the upper surface of the adjacent layer to expose the semiconductor substrate.

23. The method of claim 22, wherein upper portions of the dielectric extend less than approximately 500 angstroms above the upper surface of the semiconductor substrate subsequent to said etching the upper surface.

24. The method of claim 23, wherein the upper portions of the dielectric extend between approximately 300 angstroms and approximately 500 angstroms above the upper surface of the semiconductor substrate subsequent to said etching the upper surface.

25. The method of claim 22, wherein average thicknesses of upper portions of the dielectric layer extending above the semiconductor substrate and corresponding to each of the trenches differ by less than approximately 10%.

26. A semiconductor topography, comprising:

one or more trench isolation regions arranged within a semiconductor substrate; and

a plurality of layers arranged laterally adjacent to the trench isolation regions and upon the semiconductor substrate, wherein upper surfaces of the trench isolation regions are above the plurality of layers.

27. The topography of claim 26, wherein said upper surfaces are above the plurality of layers by an amount between approximately 150 angstroms and approximately 1000 angstroms.

28. The topography of claim 26, wherein said trench isolation regions comprise:

two trench isolation regions spaced a first distance from each other; and

a third trench isolation region spaced second distance from one of said two trench isolation regions, wherein no trench isolation regions are interposed between the third trench isolation region and the one of said two trench isolation regions, and wherein said second distance is greater than said first distance.

29. The topography of claim 28, wherein upper surfaces of said third trench isolation region is farther above the plurality of layers than upper surfaces of said two trench isolation regions.

30. The topography of claim 26, wherein said plurality of layers comprise:

a silicon nitride layer arranged above the semiconductor substrate; and

a silicon dioxide layer arranged upon the silicon nitride layer.